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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,953	04/11/2001	Marco Racanelli	00CON161P	3823

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,953	RACANELLI, MARCO	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-15,17-23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-15,17-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-15, 17-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccherini (U.S. 5,436,177) in view of Erdeljac et al. (U.S. 5,489,547) and Shao et al. (U.S. 6,156,602).

In reference to claim 1 and 14 Zaccherini (Fig.1-6) teaches an analogous method to form semiconductor device including polysilicon resistors and transistors including forming a layer (7) comprising polycrystalline silicon over a transistor gate region (4) and a field oxide region (5) on a substrate (2, 3); forming a doping barrier (10) above said polycrystalline silicon over said field oxide region (5); doping said layer over said transistor gate region with a dose of a first dopant (11), wherein said dose of said first dopant (11) is a dosage greater than required to result in said layer over said transistor gate region (4) having transistor gate electrical properties, wherein said first dopant (11) has a first conductivity type; removing said doping barrier (10); and doping said layer over said transistor gate region (4) and said field oxide region (5) with a second dopant (13) so as to form a high resistivity resistor in said layer (7) over said field oxide region (5), without affecting said transistor gate electrical properties, wherein said second

dopant (13) has a second conductivity type and wherein said resistor and said gate transistor region (4) are formed in a doped epitaxial layer (3) (column 3, lines 1-53).

Zaccherini fails to teach wherein said transistor gate region being situated over a well and said field oxide region not being situated over said well. However, Erdeljac et al. (Figs.8-11) teach a method to form semiconductor devices including polysilicon resistors and transistors formed on a substrate (10, 12, 18), wherein said substrate (10, 12, 18) includes a well region (18) and wherein said method includes forming resistors (32, 34, 56) over a field oxide region (20); forming a transistor region (44), wherein said transistor region (44) and said resistors (32, 34, 56) are formed in a doped epitaxial layer (12); and further teach forming gate electrode regions (50) over a well (18), wherein said field oxide region (20) having said resistors (32, 34, 56) formed therein is located away from said well (18) (column 5, line 10 – column 6, line 21). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Zaccherini and Erdeljac et al. to enable forming the gate transistors and field oxide regions of Zaccherini on the substrate of Erdeljac et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the gate electrodes and the field oxide regions of Zaccherini and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Zaccherini and Erdeljac et al. fail to teach wherein the resistor region of said polycrystalline silicon layer includes an inner portion and an outer portion and further comprises the steps of forming a silicide blocking layer in said

inner portion of said resistor region; doping said outer portion of said resistor region of said polycrystalline silicon layer with a third dopant so as to form a high-doped region in said resistor region, wherein said third dopant has said second conductivity type; and fabricating a contact region over said high-doped region in said outer portion of said resistor region of said polycrystalline silicon layer, wherein said contact region being electrically connected to said resistor region. However, Shao et al. (Figs.1-7) in a related method to form implanted regions teach forming a layer (16) comprising polycrystalline silicon over a transistor gate region and a field oxide region (12); doping the field oxide region (12) having said polycrystalline silicon therein with a dopant of a first conductivity type, thus forming a resistor region (38); forming a transistor gate region (40) by patterning the polysilicon layer (16); and, in a separate doping step, forming a blocking oxide layer (60) in an inner portion of said resistor; doping an outer portion of said resistor region (38) of said polycrystalline silicon layer (16) with a dopant of said first conductivity type so as to form a high-doped region (72, 74) in said resistor region; and fabricating a contact region (column 8, lines 9 – 20) over said high-doped region (72, 74) in said resistor region (38) of said polycrystalline silicon layer (16), said contact region (72, 74) being electrically connected to said resistor region (38) (column 4, line 20 – column 8, line 42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zaccherini and Erdeljac et al. with the teachings of Shao et al. to enable forming high doping areas and electrical contacts in the high resistivity resistor of Zaccherini and Erdeljac et al., as taught by

Shao et al., since this would result in the formation of electrical points of contact (column 8, lines 9 – 10).

In reference to claims 3-13, 15, 17-23 and 25, the combined teachings of Zaccherini, Erdeljac et al. and Shao et al. teach wherein said layer comprises polysilicon (Zaccherini, column 3, lines 1 – 6); wherein said transistor region is an NFET or an PFET (Shao et al., column 5, lines 7 – 21); wherein said field oxide region comprises silicon oxide (Zaccherini, column 2, lines 53 – 61); wherein the first dopant is an N-type dopant comprising phosphorous at a dose of approximately $1x10^{15}$ to $1x10^{16}$ atoms per square centimeter (Zaccherini, column 3, lines 23 – 32); wherein the second dopant is a P-type dopant comprising boron at a dose of approximately $1.0x10^{12}$ to $1.0x10^{15}$ atoms per square centimeter (Zaccherini, column 3, lines 44 – 53); wherein said doping barrier comprises a photoresist (Zaccherini, Fig.4); wherein the polycrystalline silicon layer includes a gate region (4) (Zaccherini, column 2, lines 46 – 60); and wherein said contact region comprises a silicide (Shao et al., column 8, lines 8 – 20).

The combined teachings of Zaccherini, Erdeljac et al. and Shao et al. fail to expressly teach wherein said first dopant is doped at a dose of approximately 6.5×10^{15} atoms per square centimeter; and wherein said second dopant is doped at a dose of 1.0×10^{15} atoms per square centimeter. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the disclosed dopant

concentration disclosed in the combined teachings of Zaccherini, Erdeljac et al. and Shao et al. to arrive at the claimed invention.

Response to Arguments

3. Applicant's arguments filed 09/21/2004 have been fully considered but they are not persuasive.

4. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Zaccherini teaches a method of forming resistor and transistor by performing the doping process disclosed in the claimed invention on a substrate. Having this in mind, Erdeljac et al. teaches a method of forming transistor and resistor regions on a substrate that includes a well region. Furthermore, Shao et al. teach forming contacts on the resistor formed on the resistor region for the further advantage of in the formation of electrical points of contact (Shao et al., column 8, lines 9 – 10). Since there is knowledge prior in the art to form transistor regions in the same regions disclosed in the claimed invention and furthermore, since there is a further advantage of forming the claimed contacts on the claimed resistor regions prior in the art, the combination of the prior art of record is proper.

5. Also, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

6. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is 571-272-2800. See MPEP 203.08.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
June 9, 2004

George Fourson
Primary Examiner